CLAIM AMENDMENTS

Please amend claims 2 and 12 as follows.

1. (Previously Presented) A radio frequency (RF) power amplifier, comprising:

a first, a second, a third, a fourth, a fifth, and a sixth transistor, each having a drain, a source, and a gate; and

a first, a second, a third, and a fourth resistor;

the drain of the first transistor directly connected to the sources of the second and third transistors and, the drain of the second transistor directly connected to the gate of the second transistor via the first resistor, the gate of the second transistor directly connected to the gate of the sixth transistor via the second resistor,

the drain of the fourth transistor directly connected to the sources of the fifth and sixth transistors and, the drain of the fifth transistor directly connected to the gate of the fifth transistor via the third resistor, the gate of the fifth transistor directly connected to the gate of the third transistor via the fourth resistor, the fourth resistor directly connected to the gate of the third transistor and the second resistor directly connected to the gate of the sixth transistor.

2. (Currently Amended) A system, comprising:

a radio frequency (RF) power amplifier; and

circuitry merged with the RF power amplifier to apply a digital signal to the RF power amplifier, the digital signal to program a conduction angle of the RF power amplifier; wherein the circuitry comprises multiple inverter branches of p-type metal oxide semiconductor (PMOS) and n-type MOS (NMOS) switches coupled to the RF power amplifier, wherein strengths of the multiple inverter branches are changed to program the conduction angle of the RF power amplifier.

3. (Canceled).

4. (Previously Presented) The system of claim 2, wherein the PMOS and NMOS inverter branches include a logical "1" state or a logical "0" state.

5. (Previously Presented) The system of claim 2, wherein the RF power amplifier includes a self-biased differential cross-coupled cascode stage.

6. (Original) The system of claim 5, wherein the RF power amplifier includes a driver stage.

7. (Original) The system of claim 2, further comprising a digital control function coupled to the RF power amplifier.

8. (Original) The system of claim 2, further comprising a digital control function coupled to the digital conduction angle tuning circuitry.

9. (Previously Presented) A radio frequency (RF) power amplifier, comprising:

a driver stage; and

a self-biased cascode stage coupled to the driver stage, the self-biased cascode stage including a first transistor, a second transistor, a third transistor, a fourth transistor, a fifth transistor, and a sixth transistor, each having a drain, a source, and a gate, the drain of the first transistor directly connected to the sources of the second and third transistors, the gate of the first transistor directly connected to the driver stage, the drain of the second transistor directly connected to the gate of the second transistor via the first resistor, and the gate of the second transistor directly connected to the gate of the fifth transistor via the second resistor.

10. (Original) The RF power amplifier of claim 9, further comprising a second driver stage coupled to the self-biased cascode stage.

11. (Original) The RF power amplifier of claim 9, wherein the driver stage is an inverter-type class B amplifier.

12. (Currently Amended) A method of operating a radio frequency (RF) power amplifier, comprising:

applying a digital signal to a radio frequency (RF) power amplifier;

programming a conduction angle of the RF power amplifier using the digital signal by adjusting strengths of multiple inverter branches of p-type metal oxide semiconductor (PMOS) and n-type MOS (NMOS) switches ~~coupling a combination of PMOS and NMOS switches to a driver stage of the power amplifier~~;

applying an analog information signal to the RF power amplifier; and

operating the RF power amplifier at the conduction angle specified by the digital signal.

13. (Canceled).